IN THE CLAIMS

Please amend the Claims as follows:

1. (previously presented) Apparatus for testing an integrated circuit, comprising:

a data source coupled to provide test signals to an integrated circuit being tested;

a plurality of relays selectively connecting the integrated circuit being tested to the apparatus;

a plurality of fan out elements coupled to receive data pulses from the relays and to distribute the data pulses to a plurality of latches; and

a strobe element associated with each latch thereby enabling each latch to transfer the data pulses from an input port to an output port of each latch.

2. (currently amended) The apparatus of claim 1, further comprising testing components of said apparatus each coupled to the receive the data pulses from one of the plurality of latches, the testing components of said apparatus receiving the data pulses at a frequency that is a fraction of the output signal frequency of the integrated circuit being tested.

3. (previously presented) The circuit network of claim 2, wherein the fraction is equal to the output frequency of the integrated circuit being tested divided by the number of the latches.

4. (currently amended) A method of testing an integrated circuit comprising the acts of:

providing an integrated circuit;

applying signals to the integrated circuit;

fanning out data pulses received from an output port of the integrated circuit tested;

distributing the data pulses each to one of a plurality of latches; and

calibrating a time at which each one of the plurality of latches is enabled.

5. (previously presented) The method of claim 4, further comprising the acts of:

measuring the time between initialization of the integrated circuit and detection of a first data pulse at an input port of a selected one of the plurality of latches;

calculating a clock frequency of the integrated circuit therefrom, and;

testing the integrated circuit after the measuring and calculating are performed.

6. (previously presented) The method of claim 4, further comprising the act of transmitting a repetitive bit stream with alternating voltage levels from the integrated circuit to calibrate a time at which each one of the plurality of latches is enabled.

7. (previously presented) The method of claim 4, further comprising the act of edge transitions at the output terminal of each one of the plurality of latches thereby to calibrate a time at which each one of the plurality of latches is enabled.